Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**N/C**

**OUT**

**TRIM**

**VIN**

**TEMP**

**GND**

**N/C**

**COMP**

**RF17X**

**MASK**

**REF**

**.072”**

**.110”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND**

**Mask Ref: RF17X**

**APPROVED BY: DK DIE SIZE .072” X .110” DATE: 3/13/20**

**MFG: MAXIM THICKNESS .015” P/N: MAX874C/D**

**DG 10.1.2**

#### Rev B, 7/1